

Bekir Yufka

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EDUCATION

Hacettepe University | *B.S. in Electrical and Electronics Engineering (GPA: 3.04)* Ankara, Turkey · Sep. 2022 – Jun. 2026

SUMMARY

Electrical and Electronics Engineer specializing in **Digital Design, FPGAs, and VLSI**. Experienced in the full **RTL-to-GDSII** flow and **Heterogeneous SoC design** with a focus on **ARM-based Processing System (PS)** integration and hardware acceleration. Particularly drawn to **high-frequency, high-speed digital design** – from multi-GHz ASIC timing closure to pushing FPGA platforms past their rated clock limits. Proven leadership in developing **custom RISC-V** architectures and implemented **ML algorithms in FPGA** systems for high-stakes competitions like Teknofest

EXPERIENCE

Run-x | *FPGA Design Candidate Engineer (Part-time)* Ankara, Turkey · Mar. 2026 – Present

- Developing **Heterogeneous SoC** applications, focusing on **PS-PL hardware-software co-design, Linux on FPGA (PetaLinux)** environments
- Executing **Multi-platform RTL development** and optimization across **Xilinx (Vivado), Intel (Quartus), and Lattice/Gowin** toolchains to ensure vendor-neutral architecture and IP portability.
- Working on **RF systems** using the **JESD204B** high-speed serial interface for data-converter-to-FPGA communication.

Aspilsan Energy | *AR-GE Electronics Design Candidate Engineer* Ankara, Turkey · Nov. 2025 – Jan. 2026

- Engineered MIL-STD-1275F compliant surge protection; designed high-side solid-state switching drivers.
- Optimized component selection (MOSFET/BJT) via extensive **LTspice** transient simulations.

Clonify Labs | *Electronic System Design Intern* Ankara, Turkey · Jan. 2025 – Feb. 2025

- Customized open-source **ANTMICRO** PCBs for a 3D scanner project; ensured compatibility with FPGA/SoC.
- Designed hardware architecture and executed Design for Manufacturing (DfM) using **Altium Designer**, integrating the system within **Linux (Ubuntu/CentOS)** workflows.

PROJECTS

SiliCore - Multi-Platform RISC-V MicroController | *Team Captain, Teknofest 2026 – 4th of 94 teams*

- Led a 4-person team to **4th place among 94 teams** with a **multi-platform RISC-V MCU**: one RTL codebase prototyped on **Gowin** and **Xilinx** FPGAs via automated **TCL** workflows, running at **180MHz** on FPGA, and integrating a lightweight custom **AI accelerator**.
- Built a **UVM-based** verification environment with **Spike-ISS** co-simulation, taking the design from RTL to hardware-in-the-loop **FPGA prototyping**.
- Hardened core IP blocks through the open-source **OpenLane/LibreLane** RTL-to-GDSII flow on the **SKY130** PDK, extending the same design from FPGA prototype to ASIC implementation.

PPA Optimized 32-bit Pipelined ALU | *Open Source Project*

- Designed a high-performance, multi-mode ALU reaching **1.66GHz** in Turbo mode; open-sourced the design for the community.
- Executed the complete **RTL-to-GDSII** flow using **Cadence Genus** and **Innovus** with the **Cadence GPD45 (45nm) PDK**.
- Achieved timing closure and area optimization through custom constraints, verifying functionality with **Cadence Xcelium**.

FireCore | *Custom RV32IM CPU Running DOOM*

- Co-developed a **multicycle RV32IM RISC-V processor** in **Verilog**, running at **100MHz** on a Gowin FPGA under a **38-state FSM** spanning fetch through writeback, capable of running the original **DOOM** from compiled C code at ~1.2 FPS.
- Built a **DMA bootloader** loading the binary from SPI flash into **DDR3** (via Gowin memory IP) through a custom prefetching/snoop-queue controller, plus **4KB L1 I/D caches** with full coherency that cut the DDR3 miss penalty from ~20 cycles to ~2.
- Integrated **HDMI output**, PS/2/UART keyboard input, memory-mapped I/O, and a hardware crash-dump mechanism for debugging.

Fhax | *FPGA Overclocking / Speed Validation*

- Pushed a 55nm Gowin FPGA to **700MHz** through aggressive custom timing constraints and clock-tree tuning.
- Achieved **1GHz** operation on an Intel/Altera **Agilex 3** device, validating the methodology across process nodes and vendors.

RISC-V-EYE | *Real-time Object Detection, Graduation Project*

- Built a real-time detection system pairing a **RISC-V** core with a fully custom **RTL AI accelerator** (hand-designed after evaluating **Vitis HLS**, **MATLAB HDL Coder**, and **hls4ml**) running the **TinyDet** model architecture on 128×128 images at **13 FPS**, using a **ping-pong buffer** strategy to overlap data transfer with compute.
- Trained detection models using **MATLAB Deep Learning Toolbox** and **Google Colab**.

ELE475 Solid-State Tesla Coil | *Power Electronics*

- Designed and fabricated a 40cm solid-state Tesla coil (**ESP32**-controlled full-bridge driver, **550kHz** center frequency) with precision **MOSFET gate driving** and active feedback control to reliably achieve high-voltage air breakdown.

SKILLS

Languages : SystemVerilog, Verilog, TCL, C/Bare metal C, Python, Assembly (RISC-V & x86), MATLAB

AI & Agentic Workflows : Agentic coding tools (Claude Code, Cursor) for RTL/firmware iteration, structured prompt engineering, and reproducible Git/Nix-based toolchains

EDA & ASIC : Cadence (Genus, Innovus, Xcelium) (GPD45), Vivado, HLS, Gowin, Lattice, Quartus/Quarta, Openlane Skywater PDK

Hardware : FPGAs, Altium Designer, LTspice, STM32Cube, Oscilloscopes, Logic Analyzers